Claims

1. Device for equalizing the charge of the serially connected capacitors belonging to a double layer capacitor (DLC), with one capacitor (C1 to Cn) in each case being assigned a single transformer (Tr1 to Trn) in each case whose secondary winding is connected by way of a single diode (D1 to Dn) to the positive terminal of the capacitor and directly to the negative terminal, and to a voltage comparator,

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in that a flyback transformer (Tr0) is provided whose primary and secondary windings are wound in phase-opposition to one another, whereby the end of winding of its primary winding is connected to the positive terminal (V+) of the double layer capacitor (DLC) and the start of winding is connected to the collector or drain terminal of a switching transistor (T1),
in that the end of winding of the secondary winding of the flyback transformer (Tr0) is connected directly to the negative terminal (V-) of the double layer capacitor (DLC), while the start of winding is connected by way of the series connection of a first diode (D0) and a second resistor (R2) to the negative terminal (V-) of the double layer capacitor (DLC),
in that a first voltage comparator (KOMP1) is provided whose inverting input is connected on the one hand to the emitter or source terminal of the switching transistor (T1) and on the other hand to a first resistor (R1) whose other terminal is connected to the negative terminal (V-) of the double layer capacitor (DLC),

in that a first AND element (UND1) is provided whose output is connected to the base or gate terminal of the switching transistor (T1) and to whose one input an external control signal (EN) is fed,
in that a second AND element (UND2) is provided whose output is connected to the other input of the first AND element (UND1), and whose one input is connected to the output of the first voltage comparator (KOMP1),
in that a second voltage comparator (KOMP2) is provided whose inverting input is connected to the connection point between the first diode (D0) and the second resistor (R2),
in that a first reference voltage (Vref1) is provided which is applied to the noninverting inputs of the first (KOMP1) and second voltage comparator (KOMP2),
in that the output of the second voltage comparator (KOMP2) is connected to the other input of the second AND element (UND2),
in that a monitoring unit (DIAG) is provided whose first input is connected to the output of the first voltage comparator (KOMP1), whose second input is connected to the output of the second voltage comparator (KOMP2), whose third input is connected to the inverting input of the second voltage comparator (KOMP2), at whose fourth input a second reference voltage (Vref2) is applied, and at whose output a status signal (ST) can be taken off,
in that the single transformers (Tr1 to Trn) are wound in-phase, whereby the start of winding of the secondary winding of each single transformer (Tr1 to Trn) is connected by way of a single diode (D1 to Dn) to the positive terminal of the single capacitor (C1 to Cn) assigned to it, while its end of winding is connected directly to the negative terminal of the single capacitor (C1 to Cn) assigned to it,

in that the primary windings of the single transformers (Tr1 to Trn) are connected in parallel, whereby the common start of winding is connected to the connection point between the first diode (D0) and the second resistor (R2) and the common end of winding is connected to the negative terminal (V-) and to the end of winding of the secondary winding of the flyback transformer (Tr0).

2. Device for equalizing the charge of the serially connected capacitors belonging to a double layer capacitor (DLC), with each capacitor (C1 to Cn) being assigned a single transformer (Tr1 to Trn) in each case whose secondary winding is connected by way of a single diode (D1 to Dn) to the positive terminal of the capacitor and directly to the negative terminal, and to a voltage comparator,

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in that an inductor (L1) is provided whose one terminal is connected to the positive terminal (V+) of the double layer capacitor (DLC) and whose other terminal is connected on the one hand to the collector or drain terminal of a switching transistor (T1),
in that a PNP transistor (T2) is provided whose base terminal is connected to the one terminal of the inductor (L1), whose emitter terminal is connected by way of a third resistor and a first diode (D0) to the other terminal of the inductor (L1), and whose collector terminal is connected by way of a second resistor to the negative terminal (V-) of the double layer capacitor (DLC),
in that a first voltage comparator (KOMP1) is provided, whose inverting input is connected on the one hand to the emitter or source terminal of the switching transistor (T1) and on

the other hand to a first resistor (R1), whose other terminal is connected to the negative terminal (V-) of the double layer capacitor (DLC),

in that a first AND element (UND1) is provided whose output is connected to the base or gate terminal of the switching transistor (T1) and to whose one input an external control signal (EN) is supplied,

in that a second AND element (UND2) is provided whose output is connected to the other input of the first AND element (UND1) and whose one input is connected to the output of the first voltage comparator (KOMP1),

in that a second voltage comparator (KOMP2) is provided whose inverting input is connected to the connection point between the collector of transistor (T2) and the second resistor (R2),

in that a first reference voltage (Vref1) is provided which is applied to the noninverting inputs of the first (KOMP1) and second voltage comparator (KOMP2),

in that the output of the second voltage comparator (KOMP2) is connected to the other input of the second AND element (UND2),

in that a monitoring unit (DIAG) is provided whose first input is connected to the output of the first voltage comparator (KOMP1), whose second input is connected to the output of the second voltage comparator (KOMP2), whose third input is connected to the inverting input of the second voltage comparator (KOMP2), at whose fourth input a second reference voltage (Vref2) is applied, and at whose output a status signal (ST) can be taken off,

in that the single transformers (Tr1 to Trn) are wound in-phase, whereby the start of winding of the secondary winding of each single transformer (Tr1 to Trn) is connected by way of a single diode (D1 to Dn) to the

positive terminal of the single capacitor (C1 to Cn) assigned to it, while its end of winding is connected directly to the negative terminal of the single capacitor (C1 to Cn) assigned to it, and

in that the primary windings of the single transformers (Tr1 to Trn) are connected in parallel, whereby the common start of winding is connected to the connection point between the first diode (D0) and the third resistor (R3) and the common end of winding is connected to the positive terminal (V+) of the double layer capacitor (DLC) and to the one terminal of the inductor (L1).

3. Device according to Claim 1 or 2, characterized in that the single transformers (Tr1 to Trn) and the single diodes D1 to Dn are located together with the single capacitors (C1 to Cn) in the housing of the double layer capacitor (DLC).

4. Device according to Claim 1 or 2, characterized in that the connection between the flyback transformer (Tr0) or the inductor (L1) and the single transformers is implemented by means of a two-wire bus cable.

5. Device according to Claim 1, characterized in that a first capacitor (C0) is provided, which is connected on the one hand to the cathode terminal of the first diode (D0) and on the other hand to the negative terminal (V-).

6. Device according to Claim 2, characterized in that a first capacitor (C0) is provided, which is connected on the one hand to the cathode terminal of the first diode (D0) and on the other hand to the positive terminal (V+).

7. Method for operating the device according to Claim 1 or 2,

characterized in that the operation takes place in self-controlled fashion, whereby switching transistor (T1) is made conducting as soon as an external control signal (EN) is present and as soon as the voltage at the secondary winding of the flyback transformers (Tr0) or at the inductor (L1) lies beneath a predefined value, is made nonconducting when the current flowing through the primary winding of the flyback transformer (Tr0) or through the inductor (L1) reaches a predefined value, and remains nonconducting as long as the voltage at the secondary winding of the flyback transformer (Tr0) or at the inductor (L1) exceeds a predefined value or the external control signal (EN) is not present.

8. Method according to Claim 1 or 2, characterized in that the signal duration, corresponding to the charging time, which can be measured at the output of the first voltage comparator (KOMP1) and the signal duration, corresponding to the discharging time of the flyback transformer (Tr0) or of the inductor (L1), which can be measured at the output of the second voltage comparator (KOMP2) are in each case compared with an upper and a lower limit value in the monitoring circuit (DIAG), and in that it is assumed that the double layer capacitor (DLC) and the charge equalizing circuit are in a perfect state as long as the measured values lie within the limit values, and in that the monitoring circuit (DIAG) issues a status signal (ST) corresponding to this state.

9. Method according to Claim 1 or 2, characterized in that the amplitude of the rectified discharging voltage, which can be measured during a discharging operation of the flyback

transformer (Tr0) or of the inductor (L1) after the transient reaction, is proportional to the currently lowest voltage of a single capacitor (C1 to Cn) of the double layer capacitor (DLC).

10. Method according to Claim 8 or 9, characterized
in that the amplitude of the rectified discharging voltage, which can be measured after the transient reaction, is in each case compared with an upper and a lower limit value in the monitoring circuit (DIAG),
in that it is assumed that the double layer capacitor (DLC) is in a perfect state as long as the measured values lie within the limit values, and
in that the monitoring circuit (DIAG) issues a status signal (ST) corresponding to this state.